SPECIFICATIONS

Model 4300B ADC

Analog Inputs: 16.
Connector: 17 x 2-pin front-panel connector (BERG 75789-101-34). The upper 16 pins of the left row are negative signal inputs. The upper 16 pins of the right row are connected to the common virtual ground (AC-coupled to ground). The lower two pins are connected to ground. Tapped poles are provided on the front panel with separate input cables.
Input Sensing: Charge (current integrating).
Impedance: 50 Ω ±5% within the range 0 to -60 mA DC. Outside these limits, diode protection clamping will affect input impedance.
Protection: ±25 V for 1 μsec transients; (clamping diodes to ground and -3 V).
Limitations: Maximum current for linear response: -30 mA. The linearity is degraded to typically ±(1% of reading + 0.25 pC) for -60 mA.

ANALOG-TO-DIGITAL

Resolution: Two factory options: 10 or 11 bits.
Conversion Time: Typically 10 bits in 4.8 μsec, 11 bits in 8.5 μsec.
Typical Range: 10 bits, 256 pC minus ADC pedestal; 11 bits, 480 pC minus ADC pedestal.
Sensitivity: 0.25 pC ±3%.
Integral Linearity: Typically ±0.5 pC, at worst ±(0.25% of reading + 0.5 pC) for signals of slew rate < 2 mA/nsec. For signals of slew rate 4 mA/nsec, the linearity is degraded to typically ±(1% of reading + 0.25 pC).
Differential Linearity: Typically ±10%, worst case ±20%.
Residual Pedestal: From 1 pC to 13 pC for gate width from 50 to 500 nsec, all inputs open. Adjustable with an internal potentiometer for gate width > 500 nsec. Subtracted from data by CAMAC command.
Pedestal/Gate Width Coefficient: Better than ±8 pC/μsec, typically ±3 pC/μsec.
Operating Temperature: 0° to 40°C.
Temperature Coefficient: Typically (-0.05% of reading ±0.1 count)/°C for a gate width of 500 nsec. The coefficient may vary slightly for other gate widths.
Long Term Stability: ±(0.25% of reading + 0.5 pC)/ week at constant temperature and voltage.

Model 4303 (and 4300B) TDC

SIGNAL INPUTS

Common Start (STRT)/Common Stop (STOP)/Test: Three front-panel 2-pin connectors, 100 Ω input impedance, accept complementary ECL pulses of 5 nsec minimum width.
Individual Inputs: 16 inputs in a front-panel 17 x 2-pin connector (BERG 75789-101-34), 100 Ω input impedance, accept complementary ECL pulses of 5 nsec minimum width.
Input Sensing: Time, common start or common stop.

TIME-TO-DIGITAL

Typical Range: 100 nsec to 1 μsec.
Sensitivity: 50 psec to 500 psec adjustable through a front-panel potentiometer.
Notes: Other TDC specifications are identical to the ADC specifications when applicable. The Model 3420 can be used for the same function except that it works in common stop mode only, however, because it has two functions in one module. It can save cost and CAMAC slots.

Model 4301 FERA Driver

INPUT/OUTPUT

Gate (GAI & GATE): Two inputs. Inputs are OR'd and available on the Command ECL Bus (GATE) for distribution.
Clear (CLI & CLR): Two inputs. Inputs are OR'd and available on the Command ECL Bus (CLR) for distribution.
Write Acknowledge (WAI & WAK): Two inputs. Inputs are OR'd and available on the Command ECL Bus (WAK) for distribution to the Model 4300B FERAs. The WAK may also echo the WST signal after a fixed time delay.
Write Strobe (WST & WSO): Input via Command Bus (WST) from the Model 4300B FERAs. Two outputs. For synchronous operation, the WSO signal may be connected directly to the WAI via a fixed delay cable or an active delay.
Inhibit Readout (IRI): Two inputs. Inputs are OR'd and act as a veto for the REO signal described below. Since the REO is usually connected to the first Model 4300B FERA to be read out, the IRI inhibits the readout and may be used to block the readout process until the receiver module is ready.
Readout Request (REQ, RQO & REO): Input via Command ECL Bus (REQ) from the Model 4300B FERAs. Following a fixed delay, three outputs are generated. (The delay is set to 200 nsec in the factory. It may be adjusted via the internal potentiometer RQ DEL.) The two outputs (RQO) may be used to signal a request to read out data. The third output (REO) can be vetoed by the IRI signal and is normally connected to the REN or Readout Enable input of the first Model 4300B FERA to be read out; one 2-pin connector generates differential ECL signals into 100 Ω.
ECL Data Bus (IN & OUT): 16 inputs via 17 x 2-pin connector (IN). Accepts single ended ECL signals from the ECL Ports of the Model 4300B FERAs. Generates differential ECL outputs on the 17 x 2-pin connector (OUT) for all 16 signals.
Note: Paired signals are made up of one Lemo-type connector accepting NIM signals (50 Ω input impedance), and one 2-pin connector accepting differential ECL signals (100 Ω input impedance).

Model 4302 Dual Port Fast Memory

INPUT

Data Inputs: Front-panel 34-pin connector which accepts complementary ECL signals, 100 Ω input impedance; up to 16 parallel bits can be accepted and stored in the memory word addressed at the strobe pulse arrival time; the memory address is automatically incremented by one at the end of the strobe pulse.
Strobe Veto (VETO): Front-panel 2-pin connector accepts complementary ECL pulses, 100 Ω input impedance; an input signal acts as a veto on the Write Strobe Input (WSI). Connecting the FULL output to the VETO input in adjacent Model 4302s permits simple cascading of memory units. WSI and Data Inputs must also be connected.
Write Strobe (WSI): *NIM:* two bridged Lemo-type connectors with high input impedance accept NIM level pulses; the unused input must be terminated. *ECL:* front-panel 2-pin connector accepts complementary ECL pulses; 100 Ω input impedance. The leading edge of the strobe pulse must fall inside the data pulse and must arrive at least 10 nsec after the data are valid; minimum width 20 nsec; maximum frequency 10 MHz for both NIM and ECL.
Clear Address Counter (CLR): NIM: Lemo-type connector, input impedance 50 Ω, minimum pulse width 20 nsec, accepts NIM level pulses; an input pulse resets the memory address and clears the LAM.

OUTPUT

Overflow (OVF): NIM: Lemo-type connector; generates NIM level pulses when terminated in 50 Ω. ECL: front-panel 2-pin connector generates complementary ECL levels. When the ECL port is enabled, a signal is generated as long as the memory address is equal to or exceeds the value that has been preset by switches on the side of the module; the output is active until the memory address is changed by CAMAC. The two side panel switches permit the selection of 12288, 14336, 15360, or 15872 as the overflow address.
Acknowledge (ACK): Front-panel 2-pin connector generating a complementary ECL signal; the echo of WSI with 35 nsec delay time; it is inhibited if the address counter has reached the full memory capacity.
Memory Full (FULL): Front-panel 2-pin connector generating a complementary ECL signal; active as long as the address counter has not reached the full memory capacity.

GENERAL

Packaging: RF-shielded, CAMAC #1 modules conforming with the IEEE Standard 583.
Power Requirements:

	+6 V	-6 V	+24 V	-24 V
4300B	2.1 A	2.74 A*	0.1 A	—
4301	0.1 A	1.2 A	20 mA	30 mA
4302	2.2 A	0.2 A	—	—
4303	—	1.5 A	—	0.2 A

**When all output pull-down and input matching resistors are removed, the current at -6 V is reduced to 2.4 A.*

FERA STATUS WORD REGISTER FORMAT

R1 to R8: VSN; Virtual Station Number: index source for sequential readout with zero suppression.

R9: EPS; ECL port Pedestal Subtraction: when EPS = 1, pedestals are subtracted for ECL port readout.

R10: ECE; ECL port data Compression Enable: when ECE = 1, data zeros or zeros-and-overflows are suppressed for ECL port readout.

R11: EEN; ECL port ENable: when EEN = 1, ECL port readout is permitted.

R12: CPS; CAMAC Pedestal Subtraction: when CPS = 1, pedestals are subtracted for CAMAC readout.

R13: CCE; CAMAC data Compression Enable: when CCE = 1, data zeros or zeros-and-overflows are suppressed for CAMAC sequential readout.

R14: CSR; CAMAC Sequential Readout: when CSR = 0, CAMAC random access readout is enabled; when CSR = 1, CAMAC sequential readout is enabled.

R15: CLE; CAMAC LAM Enable: when CLE = 1, LAM is enabled.

R16: OFS; OverFlow Suppression: when OFS = 1, data overflows are suppressed during ECL port readout in conjunction with ECE = 1 and for CAMAC sequential readout in conjunction with CCE = 1.

Note: The 8 bits, EPS to OFS, are set to 1 by the CAMAC Z function.